REMARKS

Claims 1-20 are pending in the application.

Claims 4-20 are withdrawn from consideration.

Claims 1-3 are rejected.

Claims 1-3 are rejected under 35 U.S.C. 103(a).

Claim 1 is currently amended.

No new matter is added.

Claims 1-3 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Objections

Claims 1-3 are objected to because of the following informalities and/or defects:

In claim 1, the term of "disposed on sidewalls" should read as: --disposed on one of two sidewalls--; otherwise the term of "resistor spacer" should be changed to: --spacers--.

Claim 1 has been amended to change "a resistor spacer" to "resistor spacers". Applicants request withdrawal of the objection.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Chang (Chang, et al.; 6,004,841).

Applicants respectfully traverse the rejections.

Claim 1 recites, among other things, "*resistor* spacers disposed on sidewalls of the resistor pattern...wherein the *resistor pattern includes a single polysilicon layer*, and wherein the resistor spacer protrudes above the resistor pattern." (Emphasis added)

Applicants respectfully submit that none of the cited references, either alone or in combination, teach or suggest these elements of claim 1.

As acknowledged in the most recent Office Action (mailed 8/1/2005), the AAPA does not disclose that the resistor pattern formed of a polysilicon layer has resistor spacers that protrudes above the resistor pattern. Nor does Chang disclose the limitations of claimed invention recited in claim 1.

In further detail, referring to FIG. 10 (which is also the cover page figure), Chang only shows *insulator* spacers 10, not resistor spacers, on three structures; a polysilicon gate

structure in NFET region 3, a polysilicon gate structure in PFET region 4, and a polysilicon bottom electrode in capacitor region 5 (col. 4, lines26-30). (Emphasis added)

Further, referring to Chang's cover page figure, the polysilicon patterns 8 are not resistor patterns. In detail, Chang clearly specifies that the disclosed polysilicon layers 8 are either part of a gate electrode (col. 4, lines 10-13) or a capacitor (col. 4, lines 26-30), which does not qualify them as being a resistor pattern, because a resistor pattern requires high resistance, i.e., low conductivity (Application, page 7, line 7).

For at least the reasons discussed above, AAPA and Chang, either alone or in combination, do not teach or suggest all of the limitations of claim 1. For example, even the insulator spacer 10 of Chang is combined with the device of AAPA or the conductive polysilicon patterns 8 of Chang, the combination would not teach or disclose the claimed invention for the reasons discussed above. Accordingly, the rejection does not present a *prima facie* case of obviousness, and claim 1 is allowable.

Claims 2-3 depend from claim 1 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 2-3 are allowable for their dependency and their own merits. Allowance of these claims is requested.

In conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-3 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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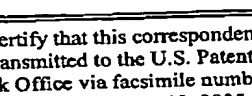

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